

WHAT IS CLAIMED IS:

1           1.    A system for synchronizing a first circuit portion  
2    operating in a first clock domain that is clocked with a  
3    first clock signal and a second circuit portion operating in  
4    a second clock domain that is clocked with a second clock  
5    signal, comprising:

6                means for generating a SYNC pulse signal based on  
7    a predetermined temporal relationship between said first and  
8    second clock signals; and

9                a clock synchronizer controller operable to  
10   generate a plurality of control signals based on said SYNC  
11   pulse signal, said clock synchronizer controller including  
12   a SYNC adjuster operable to re-position said SYNC pulse  
13   signal based on a skew between said first and second clock  
14   signals, wherein at least a portion of said plurality of  
15   control signals actuate data transfer synchronizer circuitry  
16   disposed between said first and second circuit portions.

1           2.    The system as set forth in claim 1, wherein said  
2    SYNC adjustor comprises:

3               a SYNC correct block operable to receive said SYNC  
4    pulse signal via a SYNC distributor, said SYNC correct block  
5    for correcting said SYNC pulse signal if said SYNC pulse  
6    signal has a particular clock period difference with respect  
7    to said first clock signal;

8               a ratio detector coupled to said SYNC correct block  
9    for detecting a frequency ratio relationship between said  
10   first and second clock signals;

11              a state/correct block associated with a phase  
12   detector for determining a state indicative of a phase  
13   difference between said first and second clock signals, said  
14   state/correct block operating responsive to said frequency  
15   ratio relationship detected by said ratio detector; and

16              a skew compensator operating responsive to said  
17   state to redefine a new coincident rising edge with respect  
18   to said first and second clock signals, whereby said SYNC  
19   pulse signal is re-aligned so as to correspond with said new  
20   coincident rising edges of said first and second clock  
21   signals.

1           3.    The system as set forth in claim 2, further  
2    comprising a tapline and selection block operable to drive  
3    said plurality of control signals at predetermined times  
4    based on said SYNC pulse signal.

1           4.    The system as set forth in claim 3, wherein said  
2   SYNC distributor comprises a plurality of registers.

1           5.    The system as set forth in claim 3, wherein said  
2   data transfer synchronizer circuitry comprises at least one  
3   of a CLK1-TO-CLK2 synchronizer operable to facilitate data  
4   transmission from said first circuit portion to said second  
5   circuit portion and a CLK2-TO-CLK1 synchronizer operable to  
6   facilitate data reception by said first circuit portion from  
7   said second circuit portion.

1           6.    The system as set forth in claim 5, wherein said  
2   plurality of control signals comprises a CLK1-TO-CLK2\_VALID  
3   signal provided to said first circuit portion and an NDSYNC  
4   signal operable to actuate said CLK1-TO-CLK2 synchronizer.

1           7.    The system as set forth in claim 5, wherein said  
2   plurality of control signals comprises a CLK2-TO-CLK1\_VALID  
3   signal provided to said first circuit portion and an NRSYNC  
4   signal operable to actuate said CLK2-TO-CLK1 synchronizer.

1           8. The system as set forth in claim 5, wherein each  
2 of said CLK1-TO-CLK2 and CLK2-TO-CLK1 synchronizers includes  
3 a set/reset asynchronous flip-flop.

1           9. The system as set forth in claim 5, wherein said  
2 tapline and selection block comprises a plurality of delay  
3 registers.

1           10. The system as set forth in claim 5, wherein each  
2 of said plurality of control signals is staged through at  
3 least a flip-flop.

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11. A method of synchronizing data transfer operations between two circuit portions across a clock domain boundary, comprising the steps:

generating a secondary clock signal from a primary clock signal, wherein said primary clock signal is operable to clock a first circuit portion and said secondary clock signal is operable to clock a second circuit portion;

generating a SYNC pulse signal based on a predetermined temporal relationship between said primary and secondary clock signals;

compensating for a skew between said primary and secondary clock signals and adjusting said SYNC pulse signal, if necessary; and

generating data transfer control signals at appropriate times relative to said primary and secondary clock signals based on said SYNC pulse signal to control data transfer operations between said first and second circuit portions.

12. The method as set forth in claim 11, wherein said secondary clock signal is generated by a phase-locked loop (PLL) based on said primary clock signal.

13. The method as set forth in claim 11, wherein said SYNC pulse signal is generated when a rising edge in said primary clock signal coincides with a rising edge in said secondary clock signal.

14. The method as set forth in claim 11, wherein said SYNC pulse signal is corrected if said SYNC pulse signal has a select clock period difference with respect to said primary clock signal.

15. The method as set forth in claim 11, wherein said step of compensating for a skew is comprised of the steps:  
determining a state indicative of a phase difference between said primary and secondary clock signals;  
and  
redefining a new coincident rising edge with respect to said primary and secondary clock signals based on said state.

16. The method as set forth in claim 15, wherein said new coincident rising edges with respect to said primary and secondary clock signals are redefined by adding at least an extra clock cycle when said state indicates that said primary clock signal lags with respect to said secondary clock signal by a predetermined amount.

1 17. The method as set forth in claim 15, wherein said  
2 new coincident rising edges with respect to said primary and  
3 secondary clock signals are redefined by deleting at least  
4 an extra clock cycle when said state indicates that said  
5 secondary clock signal lags with respect to said primary  
6 clock signal by a predetermined amount.

1 18. The method as set forth in claim 11, wherein said  
2 data transfer control signals are staged through a plurality  
3 of registers before being provided to data transfer  
4 synchronizer circuitry disposed between said first and second  
5 circuit portions.

1 19. The method as set forth in claim 11, wherein said  
2 primary clock signal comprises a core clock in a computer  
3 system.

1 20. The method as set forth in claim 19, wherein said  
2 secondary clock signal comprises a bus clock in a computer  
3 system.